CLAIMS

What is claimed is:

1. A vertical interconnection structure for integrated circuits of the type having first cells and a first conductor disposed in a first plane, and at least second cells and a second conductor disposed in at least a second plane substantially parallel to the first plane, said vertical interconnection structure comprising:

   a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, said antifuse being fused to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

2. A method for fabricating integrated circuits of the type having first cells and a first conductor disposed in a first plane, and at least second cells and a second conductor disposed in at least a second plane substantially parallel to the first plane, said method comprising the steps of:

   a) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

   b) subsequently fusing said antifuse to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

3. An integrated circuit fabricated by the method of claim 2.

4. A vertical interconnection structure comprising:

   a) first cells and a first conductor disposed in a first plane,

b) at least second cells and a second conductor disposed in at least a second plane substantially parallel to the first plane, and

c) a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse.

5. A vertical interconnection structure as in claim 4, wherein said antifuse comprises a tunnel junction.

6. A vertical interconnection structure as in claim 4, wherein said antifuse comprises a thin layer of insulating material.

7. A vertical interconnection structure as in claim 4, wherein said antifuse comprises a thin layer of oxide.

8. A vertical interconnection structure as in claim 4, wherein said antifuse is fused to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

9. A vertical interconnection structure as in claim 4, further comprising a substrate, said substrate being substantially parallel to said first and second planes, wherein said antifuse is disposed adjacent to said substrate.

10. A vertical interconnection structure comprising:

a) first cells and a first conductor disposed in a first plane,

b) at least second cells and a second conductor disposed in at least a second plane substantially parallel to the first plane, and

c) a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, said antifuse being fused to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

11. A vertical interconnection structure as in claim 10, wherein said antifuse is disposed adjacent to a substrate, said substrate being substantially parallel to said first and second planes.

12. A vertical interconnection structure as in claim 10, further comprising at least one redundant conductor adapted for supplying fusing current for fusing said antifuse.

13. A vertical interconnection structure as in claim 12, wherein said at least one redundant conductor is a row conductor.

14. A vertical interconnection structure as in claim 12, wherein said at least one redundant conductor is a column conductor.

15. A vertical interconnection structure as in claim 12, comprising two redundant conductors adapted for supplying fusing current for fusing said antifuse.

16. A vertical interconnection structure as in claim 15, wherein said two redundant conductors comprise a row conductor and a column conductor.

17. A vertical interconnection structure as in claim 10, further comprising at least one diode adapted for supplying fusing current for fusing said antifuse.

18. A vertical interconnection structure comprising:

a) first cells and a first conductor disposed in a first plane,

b) at least second cells and a second conductor disposed in at least a second plane substantially parallel to the first plane,

c) a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, said antifuse being fused to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor, and

d) at least one redundant conductor adapted for supplying fusing current for fusing said antifuse.

19. A method for fabricating integrated circuits, comprising the steps of:

a) disposing first cells and a first conductor in a first plane,

b) disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane,

c) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

d) subsequently fusing said antifuse to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

20. An integrated circuit fabricated by the method of claim 19.

21. The method of claim 19, wherein said vertical-interconnection forming step (c) is performed by a sub-method comprising the steps of:

i) disposing a suitable thin oxide upon said first conductor, and

ii) disposing a conductive via material upon said suitable thin oxide whereby a tunnel-junction antifuse is formed.

22. The method of claim 19, wherein said antifuse-fusing step (d) is performed by applying a voltage and current sufficient to form a continuous electrical connection.

23. The method of claim 19, wherein said antifuse-fusing step (d) is performed by applying a current through a conductor redundant to normal operation of said integrated circuits.

24. The method of claim 19, wherein said antifuse-fusing step (d) is performed by applying a current through a diode.

25. A method for fabricating integrated circuits, comprising the steps of:

a) forming and disposing first cells and a first conductor in a first plane,

b) forming and disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane,

c) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, said antifuse being formed by substeps comprising:

i) disposing a suitable thin oxide upon said first conductor, and

ii) disposing a conductive via material upon said suitable thin oxide whereby a tunnel-junction antifuse is formed, and

d) subsequently fusing said antifuse by applying a voltage and current sufficient to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

26. An integrated circuit fabricated by the method of claim 25.

27. The method of claim 25, wherein said antifuse-fusing step (d) is performed by applying a current through a conductor redundant to normal operation of said integrated circuits.

28. An integrated circuit fabricated by the method of claim 27.

29. The method of claim 25, wherein said antifuse-fusing step (d) is performed by applying a current through a diode.

30. An integrated circuit fabricated by the method of claim 29.

31. A multi-layer integrated circuit comprising:

a) first cells and a first conductor disposed in a first plane,

b) at least second cells and a second conductor disposed in at least a second plane substantially parallel to the first plane, and

c) a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, said antifuse being fused to form a continuous electrical connection for

electrically coupling said first conductor with at least said second conductor.

32. A multi-layer integrated circuit as in claim 31, comprising a multiplicity of arrays of cells, each array of said multiplicity of arrays being disposed in a layer, said vertical interconnection being adapted to address selected cells, whereby cells in a multiplicity of layers are selectively addressable.

33. A multi-layer integrated circuit as in claim 31, wherein each cell of said cells of said first and second arrays comprises a semiconductor device.

34. A multi-layer integrated circuit as in claim 31, wherein said cells of said first and second arrays are memory cells.

35. A multi-layer integrated circuit as in claim 31, wherein said multiplicity of layers comprise from two to eight layers.

36. A multi-layer integrated circuit as in claim 31, wherein said multiplicity of layers comprise from eight to twelve layers.

37. A multi-layer integrated circuit as in claim 31, wherein said multiplicity of layers comprise twelve or more layers.

38. A memory comprising:

a) first memory cells and a first conductor disposed in a first plane,

b) at least second memory cells and a second conductor disposed in at least a second plane substantially parallel to the first plane, and

c) a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, said antifuse being fused to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

39. A memory as in claim 38, comprising a multiplicity of arrays, each array of said multiplicity being disposed in a layer, whereby memory cells on a multiplicity of layers are selectively addressed.

40. A memory as in claim 39, wherein said multiplicity of layers comprise from two to eight layers.

41. A memory as in claim 39, wherein said multiplicity of layers comprise from eight to twelve layers.

42. A memory as in claim 39, wherein said multiplicity of layers comprise twelve or more layers.

43. A memory as in claim 38, wherein each memory cell of said memory cells of said first and second arrays comprises a semiconductor device.

44. A memory as in claim 38, wherein each memory cell of said memory cells of said first and second arrays comprises a storage element and a control element.

45. A memory as in claim 44, wherein said storage element of each memory cell is connected in series with said control element of that memory cell.

46. A mass storage device comprising at least one memory as recited in claim 38.

47. An integrated circuit comprising:

a) at least two arrays of cells, said cells of said arrays being disposed in first and second planes substantially parallel to each other and to a substrate, said cells of said arrays being selectively connected to first and second conductors disposed in said first and second planes, and

b) at least one vertical interconnection disposed for connecting said first and second conductors with each other, said vertical interconnection extending at least between said first and second planes and initially including an antifuse disposed adjacent to said substrate, said antifuse being selectively fused to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor, whereby said cells of said arrays are selectively addressable.

48. An integrated circuit as in claim 47, wherein said cells of said at least two arrays of cells are memory cells.

49. A method for fabricating the integrated circuit of claim 47, wherein said integrated circuit comprises a multiplicity of row conductors and a multiplicity of column conductors, at least one of said first and second conductors being coupled to one of said row conductors, said method comprising the step of selectively fusing said antifuse to form a continuous electrical connection by activating said one of said row conductors while activating all of said multiplicity of column conductors.

50. A method for fabricating the integrated circuit of claim 47, wherein said integrated circuit comprises a multiplicity of row conductors and a multiplicity of column conductors, at least one of said first and second conductors being coupled to one of said column conductors, said method comprising the step of selectively fusing said antifuse to form a continuous electrical connection by activating said one of said column conductors while activating all of said multiplicity of row conductors.

51. A memory comprising:

a) at least two arrays of memory cells, said memory cells of said arrays being disposed in first and second planes substantially parallel to each other and to a substrate, said memory cells of said arrays being selectively connected to first and second conductors disposed in said first and second planes for addressing said memory cells, and

b) at least one vertical interconnection disposed for connecting said first and second conductors with each other, said vertical interconnection extending at least between said first and second planes and initially including an antifuse disposed adjacent to said substrate, said antifuse being selectively fused to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor, whereby said memory cells of said arrays are selectively addressable.

52. A mass storage device comprising at least one memory, said at least one memory comprising:

a) at least two arrays of memory cells, said memory cells of said arrays being disposed in first and second planes substantially parallel to each other and to a substrate, said memory cells of said arrays being selectively connected to first and second conductors disposed in said first and second planes for addressing said memory cells, and

b) at least one vertical interconnection disposed for connecting said first and second conductors with each other, said vertical interconnection extending at least between said first and second planes and initially including an antifuse disposed adjacent to said substrate, said antifuse being selectively fused to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor, whereby said memory cells of said arrays are selectively addressable.

53. A vertical interconnection structure comprising:

a) a first set of means for wiring disposed in a first plane,

b) a second set of means for wiring disposed in a second plane generally parallel to said first plane, and

c) means for electrically coupling selected means for wiring of said first set with selected means for wiring of said second set, said means for electrically coupling including at least one vertical interconnection disposed for connecting said first and second means for wiring with each other, said vertical interconnection extending at least between said first and second planes and initially including an antifuse disposed adjacent to said substrate, said antifuse being selectively fused to form a continuous electrical connection for electrically coupling said first means for wiring with at least said second means for wiring.

54. A method for fabricating integrated circuits, said method comprising the steps of:

a) disposing first cells and a first conductor in a first plane,

b) providing a multiplicity of row conductors and a multiplicity of column conductors,

c) disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane, at least one of said

first and second conductors being coupled to one of said multiplicity of row conductors,

d) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

e) subsequently fusing said antifuse to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor by activating said one of said multiplicity of row conductors and all of said multiplicity of column conductors.

55. An integrated circuit fabricated by the method of claim 54.

56. The method of claim 54, further comprising selectively repeating said fusing step (e) for each selected row conductor of said multiplicity of row conductors.

57. An integrated circuit fabricated by the method of claim 56.

58. A method for fabricating integrated circuits, said method comprising the steps of:

a) disposing first cells and a first conductor in a first plane,

b) providing a multiplicity of row conductors and a multiplicity of column conductors,

c) disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane, at least one of said first and second conductors being coupled to one of said multiplicity of column conductors,

d) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

e) subsequently fusing said antifuse to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor by activating said one of said multiplicity of column conductors and all of said multiplicity of row conductors.

59. An integrated circuit fabricated by the method of claim 58.

60. The method of claim 58, further comprising selectively repeating said fusing step (e) for each selected column conductor of said multiplicity of column conductors.

61. An integrated circuit fabricated by the method of claim 60.

62. A method for fabricating integrated circuits, comprising the steps of:

a) disposing first cells and a first conductor in a first plane,

b) providing at least one redundant row conductor and at least one redundant column conductor,

c) disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane,

d) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

e) subsequently fusing said antifuse by supplying to at least one of said at least one redundant row conductor and said at least one redundant column conductor sufficient voltage and current to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

63. An integrated circuit fabricated by the method of claim 62.

64. The method of claim 62, further comprising selectively repeating said fusing step (e) for each selected vertical interconnection.

65. An integrated circuit fabricated by the method of claim 64.

66. The method of claim 62, wherein said first and second cells are each disposed in arrays having array edges, further comprising the step of disposing said at least one redundant row conductor and at least one redundant column conductor adjacent to said array edges of said arrays.

67. An integrated circuit fabricated by the method of claim 66.